

Currently Pending Claims

The following Claims 1-9 remain as originally filed, **except** Claim 6 which has been **amended** to include a missing word.

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- 1.(original) A method of testing a memory under test on a memory tester, the method comprising
2 the steps of:
- (a) applying the same sequence of transmit vectors to the memory under test and to a work
4 memory within the memory tester, the sequence of transmit vectors causing the storing
of test pattern data within the memories to which it is applied; and
- (b) subsequent to step (a), comparing the test pattern data content of the memory under
6 test with the test pattern data content of the work memory.
- 2.(original) A method as in claim 1 wherein the same sequence of transmit vectors is an instance
2 of that sequence that is applied simultaneously to the memory under test and to the work memory.
- 918 3.(original) A method as in claim 1 wherein the same sequence of transmit vectors is separate
instances of that sequence that are applied at different times to the memory under test and to the work
memory.
- 4.(original) A method as in claim 1 wherein the work memory is a selectable portion of an interior
2 test memory within the memory tester.
- 5.(original) A method as in claim 4 further comprising the step of interleaving work memory
2 transactions among banks of DRAM.
- 6.(amended) A method as in claim 4 further comprising the step of storing comparison results from
2 step (b) in an error catch memory that is a portion of an interior test memory within the memory tester.

7.(original) A method as in claim 6 further comprising the step of interleaving error catch memory
2 transactions among banks of DRAM.

8.(original) A method as in claim 4 wherein the interior test memory is comprised of a plurality of
2 memory sets and the selectable portion is a segment of a memory set.

9.(original) A method as in claim 8 further comprising the step of storing comparison results from
2 step (b) in an error catch memory that is a portion of a memory set different than the memory set of which
the work memory is a segment.

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